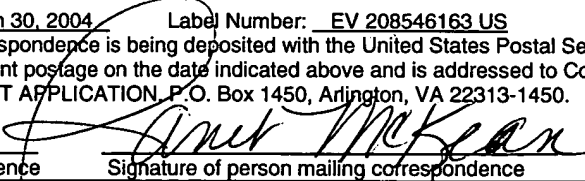


Certificate of Mailing	
Date of Deposit <u>March 30, 2004</u>	Label Number: <u>EV 208546163 US</u>
I hereby certify under 37 CFR 1.10 that this correspondence is being deposited with the United States Postal Service as " Express Mail Post Office to Addressee " with sufficient postage on the date indicated above and is addressed to Commissioner of Patents, MAIL STOP PATENT APPLICATION, P.O. Box 1450, Arlington, VA 22313-1450.	
Janet F. McKean	
Printed name of person mailing correspondence	Signature of person mailing correspondence

APPLICATION
FOR
UNITED STATES LETTERS PATENT

APPLICANT : Deenesh Padhi
Mehul Naik
Girish A. Dixit
Srinivas Gandikota
Suketu A. Parikh

TITLE : SELECTIVE METAL ENCAPSULATION SCHEMES

SELECTIVE METAL ENCAPSULATION SCHEMES

Inventors: Deenesh Padhi, Srinivas Gandikota, Mehul Naik, Suketu A. Parikh,
Girish A. Dixit

Related Applications

[0001] This application claims priority under 35 U.S.C. § 119(e) to United States
provisional application Serial No. 60/475,351, filed June 3, 2003, which is incorporated herein
by reference.

Field of the Invention

[0002] The present invention relates generally to semiconductor manufacturing, and
more particularly to systems and methods for the deposition of barrier film layers on a
conductive feature of the device.

Background of the Invention

[0003] A common goal in the integrated circuit (IC) industry is to place more conductive
circuitry into a smaller substrate surface area. Recent improvements in circuitry of ultra-large
scale integration (ULSI) on semiconductor substrates indicate that future generations of
semiconductor devices will require sub-quarter micron (or less) multilevel metallization. The
multilevel interconnects that lie at the heart of this technology require planarization of
interconnect features formed in high aspect ratio apertures, including contacts, vias, lines and
other features. One example of the use of such multilevel metallization is in “dual damascene”
processing, in which two channels of conductive materials are positioned in vertically separated
planes perpendicular to each other and interconnected by a vertical “via” at their closest point.

[0004] Currently, copper and its alloys have become the metals of choice for ULSI
technology because copper has a lower resistivity than aluminum, (1.7 $\mu\Omega$ -cm compared to 3.1

$\mu\Omega$ -cm for aluminum), a higher current carrying capacity, and significantly higher electromigration resistance. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increased device speed. Further, copper has a good thermal conductivity and is available in a highly pure state.

[0005] However, copper readily forms copper oxide when exposed to atmospheric conditions or environments outside of processing equipment. Metal oxides can result in an increase the resistance of metal layers, become a source of particle problems, and reduce the reliability of the overall circuit.

[0006] One known solution is to deposit a passivating layer or an encapsulation layer such as a dielectric material on the metal layer to prevent metal oxide formation. However, the high dielectric constant of the dielectric material increases the interlayer capacitance in multilayer environments. Furthermore, the electromigration of copper in dielectric materials is unacceptably high.

[0007] Cobalt and cobalt alloys, which are conductive (low dielectric constant) and are good barriers to electromigration of copper, have been used for passivating copper. Cobalt may be deposited by electroless deposition techniques on copper. However, copper does not satisfactorily catalyze or initiate deposition of materials from electroless solutions. It is possible to activate the copper surface to cobalt deposition by first depositing a catalytic material, such as palladium, on the copper surface. Cobalt is then selectively deposited by electroless plating onto the catalytic material. However, deposition of the catalytic material may require multiple steps or the use catalytic colloidal compounds. Catalytic colloidal compounds, and colloidal palladium materials in particular, adhere to dielectric materials and result in the undesired, excessive, and non-selective deposition of the catalyst material on the substrate surface.

Alternatively, palladium can be deposited selectively on copper surfaces by a displacement mechanism in which palladium replaces a thin layer of the exposed copper on the wafer surface. However, common semiconductor fabrication methods invariably leave copper atom contaminants on the wafer surface, so that palladium is deposited on undesired locations, e.g., dielectric surfaces, as well as desired locations, e.g., conductive metal feature. In the subsequent step of cobalt deposition, cobalt is electrolessly deposited wherever palladium is present, leading to the non-selective deposition of cobalt.

[0008] Non-selective deposition of passivation material may lead to surface contamination, unwanted diffusion of conductive materials into dielectric materials, and even device failure from short circuits and other device irregularities.

[0009] There is a need for methods and systems for deposition of passivation materials that eliminate or minimize their non-selective deposition.

Summary of the Invention

[0010] In one aspect of the methods and systems of the present invention, a sacrificial protective layer is used to prevent stray electroless deposition of a conductive passivating layer on a substrate surface. In one or more embodiments, the protective layer is deposited onto a substrate surface having at least one conductive element, and the protective layer is processed to expose the conductive element of the substrate surface. A conductive passivating layer is then deposited, e.g., electrolessly, on the exposed conductive element(s) of the substrate. The sacrificial protective layer prevents nucleation of the passivating layer on the substrate surface during deposition of the passivating layer. Any undesired deposition of passivation material on

areas other than the conductive element(s), e.g., on the protective layer, is eliminated with the removal of the protective layer.

[0011] In one or more embodiments, the protective layer is an organic material, such as photoresist, amorphous carbon, a dielectric material, or an etch stop material. In one or more embodiments, the method includes providing one or more intermediate layers disposed between the substrate surface and the protective layer.

[0012] One or more embodiments of the present invention contemplate the deposition of an intermediate layer onto the substrate surface prior to deposition of the protective layer.

[0013] In another aspect of the invention, a method of processing a semiconductor substrate to encapsulate a conductive element is provided. The method includes the steps of depositing a metallic passivating layer onto a substrate surface comprising a conductive element, masking the passivating layer to protect the underlying conductive element of the substrate surface, etching the unmasked passivating layer to expose the underlying intermediate layers or substrate surface, and removing the mask from the passivating layer after etching.

[0014] The methods and systems of the present invention provide a semiconductor device having a conductive element selectively encapsulated by a metallic passivating layer. The passivating layer interface with the conductive element is of low capacitance. The passivating layer also provides an effective barrier to electromigration of copper into adjacent dielectric regions. Significantly, the surface of the substrate is substantially free of stray electrolessly deposited passivation material, which reduces the incidence of surface contamination, device failure from short circuit, and other device irregularities.

Brief Description of the Drawing

[0015] Various objects, features, and advantages of the present invention can be more fully appreciated with reference to the following detailed description of the invention when considered in connection with the following drawings, in which like reference numerals identify like elements. The following drawings are for the purpose of illustration only and are not intended to be limiting of the invention, the scope of which is set forth in the claims that follow.

[0016] Figure 1 is a flow chart illustrating steps undertaken in selective metal encapsulation schemes according to one or more embodiments of the present invention;

[0017] Figures 2-4 are schematic illustrations of exemplary deposition processes for the selective deposition of a conductive passivating layer according to one or more exemplary embodiments of the present invention;

[0018] Figure 5 is a flow chart illustrating the steps undertaken in selective metal encapsulation schemes according to one or more embodiments of the present invention; and

[0019] Figure 6 is a schematic illustration of an exemplary integration scheme for deposition of a selective metal encapsulation layer according to one or more embodiments of the present invention.

Detailed Description of the Invention

[0020] The words and phrases used herein should be given their ordinary and customary meaning in the art by one skilled in the art unless otherwise further defined.

[0021] “Substrate surface” as used herein refers to a layer of material that serves as a basis for subsequent processing operations. For example, a substrate surface may contain one or more “conductive elements,” such as aluminum, copper, tungsten, or combinations thereof, and may form part of an interconnect feature such as a plug, via, contact, line, wire, and may also form part of a metal gate electrode. A substrate surface may also contain one or more nonconductive materials, such as silicon, doped silicon, germanium, gallium arsenide, glass, and sapphire. The substrate surface may also contain one or more low k materials such as carbon-doped oxides, porous low k materials such as organic low k and inorganic low k materials and hybrids thereof, or air-gap structures.

[0022] The term “about” is used herein to mean approximately, in the region of, roughly or around. When the term “about” is used in conjunction with a numerical range, it modifies that range by extending the boundaries above and below the numerical values set forth. In general, the term “about” is used herein to modify a numerical value above and below the stated value with a variance of 10%.

[0023] Figure 1 is a flow chart illustrating an exemplary processing sequence **100** undertaken in depositing a conductive passivating layer according to one or more embodiments of the present invention.

[0024] In step **110** in Figure 1, a substrate surface is prepared for deposition of the passivating layer. The surface can be treated to remove surface contaminants using materials

removal and/or cleaning techniques known in the art. Exemplary materials removal techniques include chemical mechanical polishing (CMP) and etching. Wet etching techniques using HF solution and dry etch techniques using HF vapor are suitable for removing dielectric materials, such as silicon oxide, from the substrate surface. Other etching techniques include downstream or remote plasma etching using a hydrogen and water plasma, or a hydrogen plasma and in situ etch processes using hydrogen, hydrogen and nitrogen, or ammonia to remove metal oxides from the substrate surface. CMP is suitable for removal of various materials, including metals and dielectric materials. Other exemplary surface treatments include ultrasonication and cleaning with an acidic solution to remove metal oxides and other contaminants from the substrate surface. The exposed conductive feature(s) can also be rinsed with distilled water to remove residual contaminants from the surface treatment process.

[0025] In step 120 of Figure 1, a sacrificial protective layer is deposited on the substrate surface. The protective layer can be any material that is compatible with the semiconductor fabrication process and that is unaffected by the subsequent deposition of a passivating layer. Exemplary materials for the protective layer include dielectrics, such as SiN, SiC, SiOC/SiC, and SiCN, photoresist, and organics such as amorphous carbon. The protective layer is deposited using known techniques such as chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), spin-on deposition and physical deposition processes, e.g., sputtering. The thickness of the protective layer can vary depending upon the materials used and the methods of material deposition and removal. Exemplary layer thicknesses are in the range of about 100 Å to about 5000 Å. With advances in deposition technology, such as atomic layer deposition, further reductions in film thickness are anticipated.

1 **[0026]** In step **130** of Figure 1, the protective layer is processed to remove materials
2 above the underlying conductive element(s) so as to expose the conductive element in the
3 underlying substrate surface. Conventional masking and materials removal techniques known in
4 the art can be used. Etching is a common technique used for the selective removal of material.
5 Before etching begins, a wafer is coated with photoresist and exposed to a circuit pattern (or
6 other pattern corresponding to the conductive element) during photolithography. Etching
7 removes material only from areas dictated by the photoresist pattern. The photoresist can be a
8 positive photoresist, in which case the exposed areas of a positive resist film are removed by the
9 process of development. Alternatively, the photoresist can be a negative photoresist, in which
10 case the mask pattern is a negative of the underlying conductive layer structure and the
11 unexposed areas of the resist film are removed by the process of development.

12 **[0027]** The exposed protective layer is then etched to selectively remove the protective
13 layer and expose the underlying conductive element. The etching technique is selective to the
14 material of the protective layer and can be a dry etch such as HF vapor or reactive ion etch (RIE)
15 with CHF_3/O_2 or plasma etch as described above. Plasma etching is performed by applying an
16 electrical field to a gas containing a chemically reactive element, thereby generating reactive ions
17 that can remove (etch) materials very rapidly. It also gives the chemicals an electric charge,
18 which directs them toward the wafer vertically. This allows vertical etching profiles, which is
19 desired in selective exposure of the features of the underlying substrate surface.

20 **[0028]** In the next step **140**, it is contemplated by one or more embodiments of the
21 present invention that an initiation layer can be deposited on the substrate surface to initiate the
22 electroless deposition process. The initiation layer can be a noble metal and is typically very

thin, e.g., only a few monolayers thick. The initiation layer generally forms selectively on the exposed conductive element by displacement of the noble metal for the conductive metal, or can be deposited as colloidal palladium. Although the displacement process is selective for the conductive metal, there typically is some stray deposition occurring on the nonconductive surfaces, e.g., the protective layer. The substrate is then rinsed to remove the displacement solution.

[0029] A conductive passivating layer then is selectively electrolessly deposited on the initiation layer in step **150** of Figure 1. The conductive material used as the passivating layer is generally a metal that does not form a solid solution with copper or other conductive metals, such as ruthenium, tantalum, tungsten, cobalt, palladium, nickel, tin, titanium, molybdenum, platinum, iron, and niobium and their alloys. In one or more embodiments, the passivating conductive metal is cobalt or a cobalt alloy. In one or more other embodiments, the passivating layer is deposited directly onto the conductive element (step **150**), without the need to first deposit an initiation layer (step **140**). Electroless deposition processes for certain cobalt alloys, using boron-containing reducing agents, permit electroless deposition of metal without the need for an initiation layer.

[0030] At least a portion of the protective layer is removed in step **160** of Figure 1 to remove any undesired passivation material at nucleation sites outside of the conductive element area. In one or more embodiments, a portion of the thickness of the protective layer is removed to ensure the removal of stray electroless deposition on the protective coating. In other exemplary embodiments, the entire protective layer is removed to expose the underlying layer, which may be the substrate surface or an intermediate layer.

[0031] The protective layer is removed or lifted using materials removal techniques known in the art. Exemplary, non-limiting materials removal techniques include chemical mechanical polishing (CMP), etching and ashing, e.g., plasma ashing. Reactive ion etching using CHF_3/O_2 , wet etch techniques using HF solution, or dry etch techniques using HF vapor, are suitable for removing dielectric materials. Other etching techniques include downstream or remote plasma etching using a hydrogen and water plasma or a hydrogen plasma and in situ etch processes using hydrogen, hydrogen and nitrogen or ammonia. Wet etching and ashing can be used for the removal of carbon-containing layers, such as amorphous carbon and photoresist. The appropriate technique depends upon the composition of the material being removed. The exposed conductive feature also can be rinsed with distilled water to remove residuals from the materials removal process.

[0032] The process provides a conductive element having a conductive passivating layer selectively deposited thereon. Elsewhere, the substrate surface is free of unwanted conductive material. In exemplary embodiments, other than the deposited passivating layer, the substrate is returned to its original state prior to deposition of the passivating layer and is ready for further processing.

[0033] The electroless deposition process is described in greater detail below. Additional information regarding electroless deposition technology, generally, is found in co-pending United States application serial number 10/117,712, entitled "Electroless Deposition Methods" and co-pending United States application serial number 10/284,855, entitled "Post Rinse To Improve Selective Deposition Of Electroless Cobalt On Copper For ULSI Application," both of which are commonly owned and are incorporated by reference herein.

[0034] Electroless deposition is generally defined herein as deposition of a conductive material generally provided as charged ions in a bath over an active surface to deposit the conductive material by chemical reduction in the absence of an external electric current. Electroless deposition typically involves exposing a substrate to a solution by immersing the substrate in a bath or by spraying the solution over the substrate.

[0035] In one or more embodiments, an initiation layer may be formed on the exposed conductive elements by deposition of a noble metal in step **140**. Embodiments of the present invention also contemplate the use of noble metals, such as gold, silver, iridium, rhenium, rhodium, rhenium, ruthenium, palladium, platinum, osmium, and combinations thereof. In one or more embodiments, the noble metal is selected from the group of palladium, platinum, or combinations thereof. The noble metal is deposited from an activation solution containing at least a noble metal salt and an inorganic acid. Examples of noble metal salts include palladium chloride (PdCl_2), palladium sulfate (PdSO_4), palladium ammonium chloride, and combinations thereof. Examples of inorganic acids include hydrochloric acid (HCl), sulfuric acid (H_2SO_4), hydrofluoric acid (HF) and combinations thereof. Alternatively, inorganic acids, such as carboxylic acids including acetic acid (CH_3COOH), may be used in the activation solution for the initiation layer.

[0036] In one or more embodiments of the present invention, displacement of the exposed conductive element, e.g., copper, by a noble metal, e.g., palladium, is carried out as follows. In a displacement plating process, wafers with an exposed copper surface are immersed in a bath containing dissolved ions of a metal more noble than copper. With simple immersion, the copper dissolves, i.e., is oxidized, and a film of the more noble metal deposits, i.e., is

1 reduced, to thereby displace atoms of copper with the noble metal. Displacement is selective to
2 copper and the coating thickness is self-limiting. Depending on the porosity of the copper, the
3 noble metal may be up to a few monolayers thick.

4 **[0037]** The noble metal salt may be in the deposition solution at a concentration between
5 about 20 parts per million (ppm) and about 20 g/liter. The concentration of the metal salt may
6 also be described as a volume percent with 1 vol% corresponding to about 40 ppm. The
7 inorganic acid is used to provide an acidic deposition composition, for example, at a pH of about
8 7 or less. A pH level between about 1 and about 3 has been observed to be effective in
9 displacement deposition of the noble metals from the activation solution. An acidic solution has
10 also been observed to be effective in removing or reducing oxides, such as metal oxides
11 including copper oxides, from the metal or dielectric surface of the substrate during the
12 activation deposition process.

13 **[0038]** The activation solution for the initiation layer is generally applied to the substrate
14 surface for between about 1 second and about 300 seconds at a composition temperature between
15 about 15°C and about 80°C. The activation solution is generally provided at a flow rate between
16 about 50 ml/min and about 2000 ml/min. In one aspect a total application of about 120 ml and
17 about 200 ml of activation solution was provided to deposit the activation layer. The activation
18 solution generally provides for the deposition of a noble metal to a thickness of about 50 Å or
19 less, such as about 10 Å or less. The initiation layer may be continuous or discontinuous.

20 **[0039]** An example of an activation solution composition for depositing the initiation
21 material includes about 3 vol% (120 ppm) of palladium chloride and sufficient hydrochloric acid

to provide a pH of about 1.5 for the composition, which is applied to the substrate surface for about 30 seconds at a flow rate of about 750 ml/min at a composition temperature of about 25°C.

[0040] In other embodiments, the initiation layer is formed by exposing the exposed conductive materials to a borane-containing composition in step 140. The borane-containing composition forms a metal boride layer selectively on the exposed conductive metals, which provides catalytic sites for subsequent electroless deposition processes.

[0041] The borane-containing composition includes a borane reducing agent. Suitable borane-containing reducing agents include alkali metal borohydrides, alkyl amine boranes, and combinations thereof. Examples of suitable borane-containing reducing agents include sodium borohydride, dimethylamine borane (DMAB), trimethylamine borane, and combinations thereof. The borane-containing reducing agent comprises between about 0.25 grams per liter (g/L) and about 6 g/L of the boron-containing composition. The borane-containing composition may additionally include pH-adjusting agents to provide a pH of between about 8 and about 13. Suitable pH adjusting agents include potassium hydroxide (KOH), sodium hydroxide (NaOH), ammonium hydroxide, ammonium hydroxide derivatives, such as tetramethyl ammonium hydroxide, and combinations thereof.

[0042] The conductive element is generally exposed to the borane-containing composition between about 30 seconds and about 180 seconds at a composition temperature between about 15°C and about 80°C. The borane-containing composition may be delivered to the substrate at a flow rate between about 50 ml/min and about 2000 ml/min. In one aspect a total application of about 120 ml and about 200 ml of the borane-containing composition was provided to form the initiation layer of a metal boride compound.

[0043] An example of a borane-containing composition for forming the layer includes about 4 g/L of dimethylamine borane (DMAB) and sufficient sodium hydroxide to provide a pH of about 9 for the composition, which is generally applied to the substrate surface for about 30 seconds at a flow rate of about 750 ml/min at a composition temperature of about 25°C.

[0044] A rinsing agent, typically deionized water, is then applied to the substrate surface to remove any solution used in forming the initiation layer.

[0045] A metallic passivating layer is deposited by an electroless process on the initiation layer in step **150**. In one or more embodiments of the present invention, the metal passivating layer comprises cobalt or a cobalt alloy. Cobalt alloys include cobalt-tungsten alloy, cobalt-phosphorus alloy, cobalt-tin alloys, cobalt-boron alloys, including ternary alloys, such as cobalt-tungsten-phosphorus and cobalt-tungsten-boron. One or more embodiments of the present invention also contemplate the use of other materials, including nickel, tin, titanium, tantalum, tungsten, molybdenum, platinum, iron, niobium, palladium, platinum, and combinations thereof, and other alloys including nickel cobalt alloys, doped cobalt and doped nickel alloys, or nickel iron alloys, to form the metal layer as described herein.

[0046] In one or more embodiments of the present invention, the metallic passivation material is deposited from an electroless solution containing at least a metal salt and a reducing agent. The electroless solution may further include additives to improve deposition of the metal. Additives may include surfactants, complexing agents, pH adjusting agents, or combinations thereof.

[0047] Suitable metal salts include chlorides, sulfates, sulfamates, or combinations thereof. An example of a metal salt is cobalt chloride. The metal salt may be in the electroless solution at a concentration between about 0.5 g/L and about 30 g/L.

[0048] Cobalt alloys, such as cobalt-tungsten may be deposited by adding tungstic acid or tungstate salts including sodium tungstate, and ammonium tungstate, and combinations thereof for tungsten deposition. Phosphorus for the cobalt-tungsten-phosphorus deposition may be formed by phosphorus-containing reducing agents, such as hypophosphite. Cobalt alloys, such as cobalt-tin may be deposited by adding stannate salts including stannic sulfate, stannic chloride, and combinations thereof. The additional metals salts, for example, for tungsten and tin, may be in the electroless solution at a concentration between about 0.5 g/L and about 30 g/L.

[0049] Suitable reducing agents include sodium hypophosphite, hydrazine, formaldehyde, and combinations thereof. The reducing agents have a concentration between about 1 g/L and about 30 g/L of the electroless solution. For example, hypophosphite may be added to the electroless solution at a concentration between about 15 g/L and about 30 g/L.

[0050] The reducing agents may also include borane-containing reducing agents, such as sodium borohydride, dimethylamine borane (DMAB), trimethylamine borane, and combinations thereof. The borane-containing reducing agent comprises between about 0.25 grams per liter (g/L) and about 6 g/L of the boron-containing composition. The presence of borane-containing reducing agents allow for the formation of cobalt-boron alloys such as cobalt-tungsten-boron and cobalt-tin-boron among others.

[0051] The metal electroless solutions described herein are generally applied to the substrate surface for between about 30 seconds and about 180 seconds at a composition

temperature between about 60°C and about 90°C. The electroless solution is generally provided at a flow rate between about 50 ml/min and about 2000 ml/min. In one embodiment of the present invention, a total application of between about 120 ml and about 200 ml of electroless solution was provided to deposit the electroless layer. The electroless solution generally provides for the deposition of a metal layer to a thickness of about 500 Å or less, such as between about 300 Å and about 400 Å.

[0052] An example of a cobalt electroless composition for forming a cobalt layer includes about 20 g/L of cobalt sulfate, about 50 g/L of sodium citrate, about 20 g/L of sodium hypophosphite, with sufficient potassium hydroxide to provide a pH of between about 9 and about 11 for the composition, which is applied to the substrate surface for about 120 seconds at a flow rate of about 750 ml/min at a composition temperature of about 80°C. A cobalt-tungsten layer is deposited by the addition of about 10 g/L of sodium tungstate.

[0053] An example of a cobalt electroless composition for forming a cobalt layer with a borane-containing reducing agent includes about 20 g/L of cobalt sulfate, about 50 g/L of sodium citrate, about 4 g/L of dimethylamineborane, with sufficient potassium hydroxide to provide a pH of between about 10 and about 12 for the composition, which is applied to the substrate surface for about 120 seconds at a flow rate of about 750 ml/min at a composition temperature of about 80°C. A cobalt-tungsten-boron layer is deposited by the addition of about 10 g/L of sodium tungstate.

[0054] Borane-containing reducing agents in the metal electroless deposition process allow electroless deposition on exposed conductive material without the need for an initiation layer. When an initiation layer is first deposited on the substrate surface prior to the metal

electroless deposition, the process is typically performed in two processing chambers. When the metal electroless deposition process occurs without the initiation layer, such as with the use of borane-containing reducing agents in the metal electroless deposition, the electroless process can be performed in one chamber.

[0055] Additionally, the method of depositing the material from an electroless solution, whether the initiation layer or metal layer, may include applying a bias to a conductive portion of the substrate structure if available (i.e. a seed layer), such as a DC bias, during the electroless deposition process.

[0056] The initiation layer and/or metal passivating layer may be annealed (i.e., heated) at a temperature between about 100°C to about 400°C. The anneal may be performed in a vacuum or in a gas atmosphere, such as a gas atmosphere of one or more noble gases (such as Argon, Helium), nitrogen, hydrogen, and mixtures thereof.

[0057] Suitable apparatus for performing electroless deposition processes include an Electra Cu™ ECP processing platform or Link™ processing platform that are commercially available from Applied Materials, Inc., located in Santa Clara, California. The Electra Cu™ ECP platform, for example, includes an integrated processing chamber capable of depositing a conductive material by an electroless process, such as an electroless deposition processing (EDP) cell, which is commercially available from Applied Materials, Inc., located in Santa Clara, California. The Electra Cu™ ECP platform generally includes one or more electroless deposition processing (EDP) cells as well as one or more pre-deposition or post-deposition cell, such as spin-rinse-dry (SRD) cells, etch chambers, or annealing chambers.

1 **[0058]** Suitable apparatus for deposition of dielectric films are the Producer™ CVD and
2 PECVD systems, available from Applied Materials, Inc., located in Santa Clara, CA. The
3 Producer™ systems use a multichamber architecture in a design that transfers wafers in pairs to
4 process modules; each module has two identical chambers that use common vacuum and gas
5 delivery subsystems. In addition to handling the full range of conventional dielectric CVD and
6 PECVD applications, the Producer™ system deposits DARC™, damascene nitride and low k
7 films such as TEOS FSG, Black Diamond™ and BLOk™ (Barrier Low k).

8 **[0059]** Etching processes, including dry etch and plasma etch, can be carried out on an
9 eMax™ etching system available from Applied Materials, Inc., located in Santa Clara, CA. The
10 system includes a low pressure/high gas flow regime, controllable magnetic field, and high rf
11 power capability. The eMax™ system integrates etch, photoresist strip and barrier removal steps
12 on a single system. Etch rates of over 6000 angstroms/min. is possible. Wet etch or wet
13 cleaning processes can be accomplished on an Oasis Clean™ system, also available from
14 Applied Materials, Inc., CA. The apparatus uses both ultrasonic cleaning and wet chemical
15 cleaning processes to clean substrate surfaces.

16 **[0060]** A suitable integrated controller and polishing apparatus is the Mirra™ with iAPC
17 or Mirra Mesa™ with iAPC, also available from Applied Materials, Inc., CA.

18 **[0061]** Figures 2A-2E illustrate an exemplary process for selective metal encapsulation
19 of a conductive element according to one or more embodiments of the present invention. Device
20 **200** is shown in Figure 2A having a substrate **210** containing conductive element **220** therein.
21 The features of device **200** represent only a portion of the device and the actual device may
22 include additional layers and/or additional device features. Furthermore, the conductive element

1 is represented in cross-section as a trench, however, is it within the scope of the invention for the
2 conductive element to comprise a variety of shapes or forms and to perform a variety of
3 functions. By way of example only, the conductive element can be an interconnect feature such
4 as a plug, via, trench, contact, line, wire, and may also form part of a metal gate electrode. It can
5 also be a metal film covering a substantial portion of the substrate surface. The conductive
6 element is made up of a conductive material, e.g., a metal having high conductivity, for example,
7 copper.

8 **[0062]** The metallic conductive element is formed in the substrate using, for example,
9 selective electroless metallization, in which the conductive metal is catalytically deposited from
10 a metal ion solution without the application of an electrical current. Because the conductive
11 metals, and copper in particular, tend to diffuse into adjacent dielectric materials such as SiO₂, it
12 is common practice to line the via opening **220** with a diffusion barrier layer (not shown) such as
13 titanium nitride, titanium tungsten, tantalum, tantalum nitride and tungsten nitride. In addition,
14 the diffusion barrier layer is activated, for example by the deposition of a seed layer of palladium
15 or displacement reaction with copper, to promote the autocatalytic deposition of copper. Other
16 methods of metallic deposition include physical vapor deposition methods such as sputter
17 deposition from the appropriate target. CMP techniques are used to polish away unwanted
18 conductive metal and to prepare the substrate for deposition of the passivating layer.

19 **[0063]** The surface can be further treated to clean the substrate surface of contaminants
20 using techniques known in the art. Wet etching techniques using HF solution and dry etch
21 techniques using HF vapor are suitable for removing dielectric materials, such as silicon oxide,
22 from the substrate surface. Other etching techniques include downstream or remote plasma

1 etching using a hydrogen and water plasma or a hydrogen plasma and in situ etch processes
2 using hydrogen, hydrogen and nitrogen, or ammonia to remove metal oxides from the substrate
3 surface. CMP is suitable for removal of various materials, including metals and dielectric
4 materials. Other exemplary surface treatments include cleaning with an acidic solution to
5 remove metal oxides and other contaminants from the substrate surface. The exposed conductive
6 feature can also be rinsed with distilled water to remove residual contaminants from the surface
7 treatment process.

8 **[0064]** After substrate surface preparation, a sacrificial protective layer **230** is deposited
9 on the substrate surface, as is illustrated in Figure 2B. The protective layer can be deposited by
10 any method that is compatible with the device fabrication process and can be made up of any
11 material that can be incorporated into the device fabrication process without detriment to the
12 subsequent processing steps.

13 **[0065]** In exemplary embodiments, the protective layer is a photoresist, which can be
14 applied to the substrate as a spin-on layer at a thickness of about 1000 Å to about 5000 Å.
15 Subsequently, the photoresist is exposed and developed to define one or more openings **240** that
16 provides access to the underlying conductive element(s) **220**, as is shown in Figure 2C. A thin
17 layer **250** of passivation material is deposited on conductive element **220** by electroless
18 deposition as described above and as shown in Figure 2D. The passivating layer can be less than
19 about 400 Å and can have a thickness in the range of about 30 Å to about 300 Å in at least some
20 embodiments. The passivating layer may be deposited in two steps by first depositing an
21 initiation layer, followed by depositing a conductive passivating layer. Alternatively, the
22 passivating layer may be deposited in a single step directly onto the conductive element.

1 Regardless of the method of passivating layer deposition, random nucleation sites **255** of the
2 passivating metal also form on the protective layer **230**. In a subsequent step shown in Figure
3 2E, the photoresist **230** is lifted off of the substrate surface so that unwanted nucleation sites **255**
4 are removed and the passivating layer **250** remains only on the conductive element **220**. The
5 photoresist is removed by conventional processes, such as wet etch or ashing, that is selected to
6 remove the photoresist without negative effect on the underlying intermediate layer(s) or
7 substrate surface. The substrate can be cleaned using wet solvent that does not dissolve the
8 passivating layer. The device is then further processed consistent with its intended function.

9 **[0066]** The above procedure is attractive because it does not require the use of a high k
10 dielectric material adjacent to the conductive element. Low k materials, e.g., polyarylethers,
11 fluorinated polyarylethers, polyimides and fluorinated polyimides, benzocyclobutenes, carbon-
12 doped oxides, organic and inorganic porous low k materials and hybrids thereof, and the like, can
13 be directly applied to the substrate surface after completion of the processing steps set forth in
14 Figures 2A-2E to provide improved electrical isolation between adjacent conductive regions of
15 an integrated circuit that is advantageous in many semiconductor devices.

16 **[0067]** In another exemplary embodiment, the protective layer **230** is a dielectric barrier
17 layer such as an etch stop layer. Exemplary etch stop materials include SiN or SiOC available
18 from Applied Materials, Inc., located in Santa Clara, California, under the tradename Blok™.
19 The etch stop layer (or other dielectric) is deposited as a thin layer, e.g., about 50 Å, over the
20 substrate surface by, for example, PECVD or spin-on polymer deposition. Alternatively, a thick
21 layer of dielectric material is deposited and is etched or polished back to a very thin protective
22 layer, for example about 50 Å. The thinness of the protective layer is chosen to reduce the

1 amount of high k material deposited on the metallic conductive element and thereby reduce
2 interlayer capacitance. The conductive element is exposed by removing, i.e., etching, the
3 dielectric layer in those areas not protected by a photomask (not shown) to define one or more
4 openings **240** that exposes the underlying conductive element **220**, as is shown in Figure 2C. A
5 passivating layer **250** is deposited as described above. The dielectric barrier (protecting layer) or
6 at least a portion of the protecting layer is then removed along with surface contaminants **255**. In
7 one or more other exemplary embodiments, only a portion of the dielectric layer is removed
8 (sufficient to remove stray electrolessly deposited sites **255**), and additional dielectric material is
9 deposited on the remaining dielectric layer to a final thickness. The final thickness is desirably
10 low to minimize the effects of the high k material, and can be in the range of about 600 Å. The
11 device is then further processed consistent with its intended function.

12 **[0068]** In another embodiment of the present invention, the protective layer **230** is an
13 amorphous carbon layer. In one or more embodiments, the amorphous carbon layer is deposited
14 onto the substrate surface, for example, by CVD or spin-on polymer deposition to a thickness of
15 about 100 Å to about 5000 Å. The conductive element is exposed by masking the amorphous
16 carbon film and developing the photoresist to expose the underlying amorphous carbon film.
17 The carbon film is then removed, e.g., by etching, in those areas not protected by the photomask
18 (not shown) to define one or more openings **240** that exposes the underlying conductive
19 element(s) **220**, as is shown in Figure 2C. A passivating layer **250** is deposited as described
20 above. The amorphous carbon layer is then removed along with surface contaminants **255** to
21 eliminate stray electrolessly deposited passivation material (and other contaminants).
22 Amorphous carbon can be removed by ashing, plasma ashing and wet or dry chemical etching.

1 As with the use of a photoresist, the process results in the complete removal of the amorphous
2 carbon film, so that no high k dielectric material remains adjacent to the conductive elements.
3 The device is then further processed consistent with its intended function.

4 **[0069]** In another exemplary embodiment of the present invention, intermediate layers
5 may be deposited between the substrate surface and the protective layer. Figures 3A-3F
6 illustrate an exemplary process for such an integration scheme using a conductive passivating
7 layer. Device **300** is shown in Figure 3A having a substrate **310** containing a conductive element
8 **320** therein. As noted above, the features of device **300** represent only a portion of the device
9 and the actual device may include additionally layers and/or additional device features.

10 **[0070]** A sacrificial protective layer **330** is deposited on the substrate surface, as is
11 illustrated in Figure 3B. Prior to deposition of the protective layer, one or more intermediate
12 layer(s) **335** is deposited on the substrate surface. The protective and intermediate layers can be
13 any of the materials and layers described above, and can be deposited according to any of the
14 method described herein or any other conventional technique. In an exemplary embodiment, the
15 protective layer is a photoresist and the intermediate layer is a dielectric material such as an etch
16 stop.

17 **[0071]** As is shown in Figure 3B, dielectric material **335** is deposited over the substrate
18 surface **310**, e.g., by PECVD or spin-on polymer deposition, to a thickness of about 50 to about
19 1000 Å. A photoresist layer **330** then is applied to the intermediate layer as a spin-on layer at a
20 thickness of about 1000 Å to about 5000 Å. Subsequently, the photoresist is exposed and
21 developed to define one or more openings **340** that exposes the underlying intermediate layer
22 **335** above the conductive element **320**, as is shown in Figure 3C. The conductive element is

1 exposed by removing, i.e., etching, the dielectric layer in those areas not protected by a
2 protective layer **330** to define one or more openings **345** that exposes the underlying conductive
3 element **320**, as is shown in Figure 3D. In one or more embodiments of the present invention,
4 the etch is selective for the intermediate layer **335**, so that protective layer **330** is not affected by
5 the etch process. In one or more embodiments, the photomask is removed only after etching of
6 both the protective and intermediate layers.

7 **[0072]** A thin layer **350** of passivation material is deposited on conductive element **320**
8 by electroless deposition as described above and as shown in Figure 3E. The passivating layer
9 can be less than about 400 Å, and has a thickness in the range of about 30 Å to about 300 Å in
10 exemplary embodiments. The passivating layer **350** can be of the same or different thickness as
11 the dielectric layer **335**. The passivating layer may be deposited in two steps by depositing an
12 initiation layer, followed by depositing the conductive passivating layer. Alternatively, the
13 passivating layer may be deposited in a single step directly onto the conductive element.
14 Regardless of the method of passivating layer deposition, random nucleation sites **355** of the
15 passivating metal also form on the protective layer. In a subsequent step shown in Figure 3F, the
16 protective layer **330** (e.g., photoresist), including unwanted nucleation sites **355**, is lifted off of
17 the substrate surface, leaving the passivating layer **350** only on the conductive element **320**. The
18 photoresist is removed by conventional processes, such as wet etch or ashing, that is selected to
19 remove the photoresist without negative effect on the underlying dielectric materials of the
20 intermediate layer(s) or substrate surface. Upon removal of the photoresist layer, dielectric layer
21 **335** covers the remaining surface of the substrate **310**. In those embodiments where the
22 dielectric layer **335** and the passivating layer **350** are of the same thickness, a smooth planar

1 substrate surface containing the passivating layer embedded in a dielectric is obtained, as
2 illustrated in Figure 3F. The substrate can be cleaned using wet solvent that does not dissolve
3 the passivating layer. The device is then further processed consistent with its intended function.

4 **[0073]** Figures 4A-4D illustrate still another embodiment of the present invention.

5 Figure 4A shows a device **400** including a first lower layer **430** of a first dielectric material and a
6 second upper layer **440** of a second dielectric material deposited on a substrate **410**. The device
7 also includes a conductive element **420** embedded in the second dielectric/first
8 dielectric/substrate composite. The layers are deposited and processed using conventional
9 methods. The first and second materials of dielectric layers **430**, **440** are selected to have
10 different etching chemistries so that one layer is inert to etching under conditions that etch the
11 other layer. Exemplary first and second dielectric materials include organic dielectrics such as
12 organic low k materials and inorganic dielectrics such as carbon-doped oxides, SiOC, fluorine-
13 doped silicon glass (FSG), and silicon oxide-based low k materials such as Black Diamond™
14 available from Applied Materials, Inc., located in Santa Clara, CA. In an exemplary
15 embodiment, the upper dielectric layer **440** is an organic low k material and the lower dielectric
16 layer **430** is a carbon-doped oxide. In one or more embodiments, the upper and lower dielectric
17 materials are the same, and an intermediate surface is treated to alter the etching characteristics
18 of the layer. Exemplary treatments that alter etching properties of the layer include inert gas
19 plasma treatments. The surface treated substrate acts as an etch stop. The surface treatment can
20 be applied in a separate step or as an integral part of the deposition process for dielectric layers.

21 **[0074]** Referring to Figure 4B, the device is processed by CMP to remove a portion of
22 the upper dielectric layer **440** and conductive element **420** from the substrate surface. In an

1 exemplary embodiment, the dielectric layer **440** has a thickness of about 100 Å to about 400 Å
2 after CMP processing. The surface is then cleaned as described above, for example, with an acid
3 bath to remove residual traces of metal on the substrate surface. Subsequently, a passivating
4 layer is deposited on the substrate surface using electroless deposition as described herein. The
5 resultant layer forms a continuous passivating layer **450** on the conductive element and random
6 discontinuous islands **455** of passivation material on the dielectric layer **440**, as is shown in
7 Figure 4C. The device is then exposed to an etchant that selectively removes the remaining
8 traces of dielectric layer **440**. The final device includes a clean dielectric layer **430** in which a
9 conductive metal layer **450** is embedded. In one or more embodiments, the metallic passivating
10 layer (and a portion of the conductive element) may extend above the plane of the substrate
11 surface. The device is then further processed consistent with its intended function.

12 **[0075]** One or more embodiments of the present invention also contemplate methods of
13 encapsulating a conductive element using a conductive passivating layer without the need for
14 first depositing a sacrificial protective layer. According to one or more embodiments of the
15 present invention, a conductive element is encapsulated without stray electroless deposition of
16 passivating metal elsewhere on the substrate surface by depositing a layer of the passivation
17 material over the entire substrate surface or a portion thereof containing the conductive
18 element(s), masking the passivation layer to protect the underlying conductive element(s) and
19 removing the unmasked passivation material from the substrate surface to reveal the underlying
20 substrate or other underlying intermediate layers. One or more embodiments of the present
21 invention contemplate the deposition of an intermediate layer onto the substrate surface prior to
22 deposition of the metallic passivating layer. The mask is subsequently removed to obtain the

selectively encapsulated metal device, in which the surrounding substrate surface areas are substantially free of contaminants arising from the deposition of the passivating layer.

[0076] Figure 5 is a flow chart illustrating an exemplary processing sequence **500** undertaken in encapsulating a conductive element with conductive passivating layer according to one or more embodiments of the present invention.

[0077] In step **510** in Figure 5, a substrate surface is prepared as previously described by treating the substrate surface so as to expose the conductive element. The substrate surface can be treated using materials removal and cleaning techniques known in the art. Exemplary materials removal techniques include chemical mechanical polishing (CMP) and etching. Wet etching techniques using HF solution and dry etch techniques using HF vapor are suitable for removing dielectric materials, such as silicon oxide, from the substrate surface. Other etching techniques include downstream or remote plasma etching using a hydrogen and water plasma or a hydrogen plasma and in situ etch processes using hydrogen, hydrogen and nitrogen or ammonia to remove metal oxides from the substrate surface. CMP is suitable for removal of various materials, including metals. Other exemplary surface treatments include ultrasonication and cleaning with an acidic solution to remove metal oxides and other contaminants from the substrate surface. The exposed conductive feature can also be rinsed with distilled water to remove residual contaminants from the surface treatment process.

[0078] A conductive passivating layer then is deposited on the substrate surface in step **530** of Figure 5. The conductive passivation material is generally a metal that does not form a solid solution with copper or other conductive metals, such as ruthenium, tantalum, tungsten, cobalt, palladium, nickel, tin, titanium, molybdenum, platinum, iron, and niobium and their

1 alloys. In one or more embodiments, the passivating conductive metal is cobalt or a cobalt alloy.
2 One or more embodiments contemplate the deposition of the conductive passivation layer as a
3 continuous film across the substrate surface. The continuous film is deposited, for example,
4 physical deposition techniques such as sputter deposition using a suitable target.

5 [0079] In step 540 of Figure 5, the passivating layer is masked in a pattern of the
6 underlying conducting elements. The passivating layer can be masked with photoresist, which is
7 developed to remove selected areas of the photoresist film so that the underlying conductive
8 elements are protected and the surrounding dielectric regions are exposed. The photoresist can
9 be a positive photoresist, in which case the exposed areas of a positive resist film are removed by
10 the process of development. Alternatively, the photoresist can be a negative photoresist, in
11 which case the mask pattern is a negative of the underlying conductive layer structure and the
12 unexposed areas of the resist film are removed by the process of development.

13 [0080] In step 550 of Figure 5, the exposed passivating layer is then etched to selectively
14 remove the unmasked passivating layer and to expose the underlying substrate surface.
15 Exemplary etching processes for removal of cobalt includes etching at elevated temperatures,
16 e.g., of greater than 120°C, using Cl₂ gas, and including CO, CF₄ or N₂ gas for passivation. The
17 etching process is selective for the metallic passivation material and leaves the substrate surface
18 free of passivation material (and other contaminants) without deleterious effect to the substrate,
19 i.e., the dielectric regions or conductive elements of the substrate.

20 [0081] The protective mask is then removed or lifted to expose the encapsulating
21 passivating layer, as is shown in step 560. Materials removal techniques known in the art can be

1 used. Wet etching and ashing can be used for the removal of the photoresist. The device also
2 can be rinsed with distilled water to remove residuals from the materials removal process.

3 **[0082]** Figures 6A-6D illustrate an exemplary process for selective metal encapsulation
4 of a conductive element according to one or more embodiments of the present invention. Device
5 **600** is shown in Figure 6A having a substrate **610** containing conductive element **620** therein.
6 As above, the features of device **600** illustrate only a portion of the device and the actual device
7 may include additional layers and/or additional device features. The metallic conductive element
8 can be prepared as previously described or according to known methods in the art.

9 **[0083]** A thin layer **630** of passivation material is deposited as a continuous layer on
10 substrate surface **610** as shown in Figure 6B, thereby encapsulating at least the conductive
11 element **620**. The passivating layer can cover the entire substrate surface, or a selected region
12 thereof; however, the deposited passivating layer should cover at least the conductive element(s).
13 The passivating layer can be less than about 400 Å and has a thickness in the range of about 30 Å
14 to about 300 Å in some embodiments. The passivating layer can be deposited using physical
15 vapor deposition techniques such as sputtering. In sputtering, a target of a composition
16 commensurate with the desired composition of the passivating layer is bombarded with a
17 sputtering gas, typically an inert gas, to remove atoms from the target, which are then deposited
18 on the substrate surface. A suitable apparatus for sputter deposition is the Endura™ processing
19 system, available from Applied Materials, Inc., located in Santa Clara, CA.

20 **[0084]** A photoresist **640** is deposited and developed as shown in Figure 6C to mask the
21 underlying conductive element **620** of the substrate surface. The photoresist can be applied to
22 the substrate as a spin-on layer and developed using conventional techniques. The surface is

then etched as shown by arrows **650** to remove exposed passivation material **655** and to uncover the underlying regions of the substrate surface **610**. Exemplary etch process suitable for metals etching include the use of decoupled plasma source (DPS) technology. Suitable apparatus for metal etching of cobalt (or other passivating metals) includes the Centura System using Metal Etch DPS processing platform, available from Applied Materials located in Santa Clara, CA.

[0085] In a subsequent step shown in Figure 6D, the photoresist **640** is lifted off to reveal passivating layer **660** and to provide a passivating layer-encapsulated conductive element **665** in which the surrounding substrate surface is substantially free of surface contaminations.

[0086] Although various embodiments that incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that incorporate these teachings, including embodiments with numerical values and ranges differing from those set forth herein. It is appreciated that the figures and discussion herein illustrate only a portion of an exemplary semiconductor device. Thus, the present invention is not limited to only those structures described herein.

What is claimed is: